WHAT IS CLAIMED IS:

1. A memory data access structure suitable for use in a processor, comprising:

a cache memory, to store and output an instruction according to an address signal; and

a pipeline processor, for executing a plurality of processor instructions, the pipeline processor including an execution unit to perform an execution operation on the instruction input from a previous stage, and to output a result signal and a control signal, wherein the control signal is output to the cache memory, wherein

when the instruction executed by the execution unit is a branch instruction, the result signal is a target address, wherein the target address is selected to be an address signal output to the cache memory, wherein the cache memory fetches an next instruction to be executed according to the address signal;

when the execution unit is executing the branch instruction, the processor is fetching a fetch instruction from the cache memory, and when the control signal obtained after executing the branch instruction is output to the cache memory, if the fetch instruction is not stored in the cache memory, the cache memory determines whether to fetch the fetch instruction from an external memory according to the control signal.

2. The memory data access structure according to claim 1, wherein the control signal indicates whether the instruction executed in the current stage is a taken branch instruction.

3. The memory data access structure according to claim 1, further comprising a program counter to store an address of the instruction currently executed among all the instructions to be executed.

4. The memory data access structure according to claim 3, further comprising a multiplexer to receive the result signal output by the execution unit and the executed address stored in the program counter plus a set value, and to select one of the signals as the address signal.

5. A memory data access structure suitable for use in a processor, comprising

a cache memory, to store and output an instruction according to an address signal;

a pipeline processor, for executing a plurality of processor instructions, including an execution unit to perform an execution operation on an instruction transferred from a previous stage, and to output a result signal;

a branch instruction prediction mechanism, to output a predicted address according to a fetch instruction; and

a comparator, to receive the result signal and the predicted address and to output a comparison signal, wherein

when the execution unit is executing a branch instruction, the result signal is a target address, wherein the target address is selected to be an address signal output to the cache memory, wherein an next instruction to be executed is fetched according to the address signal,

when the execution unit is executing the branch instruction, the processor fetches the fetch instruction, and the result signal obtained after executing the branch instruction is transferred to the comparator, the comparator then outputs the comparison signal to the cache memory according to the result signal and the predicted address, if the fetch instruction is not stored in the cache memory, the cache memory determines whether to fetch the fetch instruction from an external memory according to the comparison signal.

6. The memory data access structure according to claim 5, wherein the comparison signal is generated after performing comparison operation upon the result signal and the predicted address.

7. The memory data access structure according to claim 5, further comprising a program counter to store an address of an instruction which is executed currently among all the instructions to be executed

8. The memory data access structure according to claim 7, comprising further a multiplexer to receive the result signal output from the execution unit, an execution address stored in the program counter plus a signal with a determined value, and the predicted address, and to select one of these signals as an address signal

9. A method of memory data access suitable for use in a processor, comprising:

providing an instruction according to an address signal;

executing the instruction to output a result signal and a control signal;

fetching a next instruction to be executed according to an address signal, wherein when the instruction is a branch instruction, the result signal is a target address, wherein the target address is selected to be the address signal output to the cache memory; and

determining whether a fetch instruction is fetched from an external memory according to the control signal when the processor is fetching the fetch instruction and the fetch instruction is not stored in the cache memory.

10. The method according to claim 9, wherein the control indicates whether the instruction currently executed is a taken branch instruction.

11. The method according to claim 9, comprising further the step of selectively outputting the result signal and an address of the instruction executed currently plus a signal with a certain value.

12. A method for memory data access suitable for use in a processor, comprising:

providing an instruction;

executing the instruction to output a result signal;

using a branch prediction mechanism to receive a fetch instruction and to output a predicted address;

comparing the result signal with the predicted address, and outputting a comparison signal, wherein

when the instruction being executed is a branch instruction, the result signal is a target address and is selected to be an address signal, the processor fetches an instruction to be executed next according to the address signal;

while executing the branch instruction, the processor fetches the fetch instruction, if the fetch instruction is not in a cache memory, according to the comparison signal, the cache memory determines whether to fetch the fetch instruction from an external memory.

13. The method according to claim 12, comprising further a step of selectively outputting one of the result signals, an address that the processor is currently processing plus a certain value, and the predicted address.

14. The method according to claim 12, wherein the comparison signal indicates whether the branch instruction predicted by the branch prediction mechanism is correct.